AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of propagating signals on programmable interconnect in a programmable logic device, the method comprising:

selecting by a selection device between source signals to drive a shared programmable interconnect portion located on the programmable logic device; and

coordinating latching of the source signals in corresponding capture devices via a time multiplexing signal generator coupled to the selection device and the capture devices.

2. (Original) The method of Claim 1, wherein the source signals are provided by a configurable logic block in the programmable logic device.

3. (Original) The method of Claim 1, wherein the source signals are provided by configurable logic blocks in the programmable logic device.

4. (Previously Presented) The method of Claim 1, wherein the capture devices are provided in a configurable logic block in the programmable logic device.

5. (Previously Presented) The method of Claim 1, wherein the capture devices are provided in configurable logic blocks in the programmable logic device.

6. (Original) The method of Claim 1, wherein the source signals include non-critical signals.

7. (Original) The method of Claim 1, wherein the source signals include critical signals.

8. (Previously Presented) The system of Claim 1, wherein the capture devices comprise latches.

9. (Previously Presented) The method of Claim 1 further comprising:

connecting the selecting device to the capture devices using a programmable interconnect point.

10. (Currently Amended) A method of propagating signals in a programmable logic device, the method comprising:

selecting by a selection device between source signals to route signals onto a shared programmable interconnect on the programmable logic device;

routing signals from the shared programmable interconnect to the capture devices through a first programmable interconnect point; and

controlling by a clock applied to the selection device and capture devices the provision of the source signals through the selection device and the capture devices.

11. (Previously Presented) The system of Claim 10, wherein the capture devices comprise latches.

12. (Previously Presented) The method of Claim 10, wherein additional programmable interconnect points connect the first programmable interconnect point to the capture devices.

13. (Currently Amended) A configured programmable logic device comprising:

a multiplexer which chooses between source signals to drive a shared programmable interconnect on the programmable logic device;

flip flops which receive the source signals from the shared programmable interconnect; and

a clock which is coupled to the multiplexer and flip flops.

14. (Previously Presented) The method of Claim 13, wherein the multiplexer is connected to the flip flops by a first programmable interconnect point.

15. (Previously Presented) The method of Claim 14, wherein additional programmable interconnect points connect the first programmable interconnect point to the flip flops.